

Nadi DMA

A 33 ns PCIe DMA engine for FPGA.

Encrypted-IP licensed. Built on the Xilinx/AMD UltraScale+ platform.

LATENCY

33 ns doorbell → completion

13 cycles @ 390.625 MHz

SUPPORTED DEVICES

UltraScale+ family

PCIe4/PCIe4C integrated block

DELIVERY

Encrypted IP

Nadi DMA is a PCIe DMA engine for FPGA that delivers a 33 ns doorbell-to-completion path — the physical floor on UltraScale+ silicon. The DMA ships as encrypted IP through the Vivado catalog, under a free evaluation license capped at ~1 million transactions and a paid production license per project.

For more info, evaluate and license, reach out at sales@siliscale.com.

HIGHLIGHTS

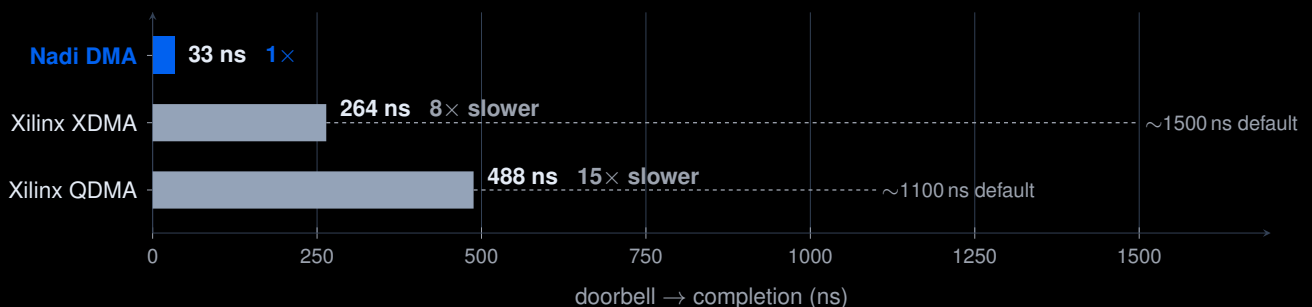
33_{ns}

Doorbell → completion

13 cycles @ 390.625 MHz

on Alveo U280, 64B frames

At 390.625 MHz, 13 cycles is the minimum for a complete doorbell → MAC → completion sequence that includes a posted-write completion.



All three measured on the same Alveo U280. XDMA and QDMA shown in their best-case tuned configuration — descriptor pre-fetch enabled, poll mode, 64-byte payload already on card, one million samples. Dashed extensions show the same products without tuning on the same card: XDMA ~1500 ns (45× Nadi), QDMA ~1100 ns (33× Nadi).

The IP comes with a Linux VFIO userspace driver. A reference design for a 10/25G and 100G network interface card is also available, with a Linux network driver and a Data Plane Development Kit (DPDK) driver.